CLAIMS

What is Claimed is:

1. A power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal functions as an input terminal of said power-up bias circuit;

a second inverter having an input terminal and an output terminal, said output terminal of said second inverter functions as the output terminal for said power-up bias circuit; and

a Schmitt Trigger circuit having an input terminal and an output terminal, wherein said input terminal of the Schmitt Trigger circuit is connected to said output terminal of said first inverter, said output terminal of said Schmitt Trigger circuit is connected to said input terminal of said second inverter, said first inverter, said second inverter and said Schmitt Trigger circuit are each in electrical communication with a voltage input terminal and ground.

2. A power-on bias circuit according to claim 1, wherein said voltage input terminal is an input/output voltage input terminal.

3. A power-on bias circuit according to claim 2, wherein said input terminal of said power-on bias circuit is further in electrical communication with a core voltage input terminal.

4. A power-on bias circuit according to claim 3, wherein said first inverter comprises a transistor of a first conductivity and a transistor of a second conductivity, a substrate and a source region of said transistor with the first conductivity are in electrical communication with said input terminal of said input/output terminal, a source and a substrate region of said transistor having the second conductivity is electrically connected to ground, a gate of said transistor with the first conductivity and the gate of said transistor with the second conductivity are electrically connected to said input

terminal of said first inverter, a drain region of said transistor with the first conductivity and a drain region of said transistor with the second conductivity are electrically connected to said output terminal of said first inverter.

5. A power-on bias circuit according to claim 4, wherein said transistor of the first conductivity is a P-type transistor, said transistor of the second conductivity is an N-type transistor.

6. A power-on bias circuit according to claim 3, wherein said second inverter comprises a transistor of a first conductivity and a transistor of a second conductivity, a substrate and a source region of said transistor having the first conductivity are electrically connected to said input terminal of the input/output terminal, a source region of said transistor having the second conductivity is electrically connected to ground, a gate of said transistor having the first conductivity and the gate of said transistor having the second conductivity are electrically connected to said input terminal of said second inverter, a drain region of said transistor having the first

conductivity and a drain region of said transistor having the second conductivity are electrically connected to said output terminal of said second inverter.

7. A power-on bias circuit according to claim 6, wherein said transistor having the first conductivity is a P-type transistor, said transistor having the second conductivity is an N-type transistor.

8. A power-on bias circuit according to claim 3, wherein said Schmitt Trigger circuit further comprises:

a first transistor having a first conductivity;

a second transistor having said first conductivity, a substrate of said second transistor having the first conductivity, a substrate and a source region of said first transistor having said first conductivity are electrically connected to said input terminal of the input/output terminal, a source region of said second transistor having the first conductivity is electrically connected to a drain region of said first transistor having said first conductivity;

a first transistor having a second conductivity;

a second transistor having said second conductivity, a gate of said first transistor having the first conductivity, a gate of said second transistor having said first conductivity, a gate of said first transistor having the second conductivity and a gate of said second transistor having said second conductivity are electrically connected to said input terminal of said Schmitt Trigger circuit, said input terminal of said Schmitt Trigger circuit is electrically connected to said output terminal of said first inverter, a substrate of said second transistor having the second conductivity, a substrate and a source region of said first transistor having said second conductivity are electrically connected to ground, a drain region of said second transistor having the second conductivity is electrically connected to a source region of said first transistor having the second conductivity;

a third transistor having said first conductivity, a source region of said third transistor having the first conductivity is electrically connected to said drain region of said first transistor having the first conductivity and said source region of said second transistor having the first conductivity, a drain region of the third transistor having the

first conductivity is electrically connected to ground, a substrate of said third transistor having the first conductivity is electrically connected to an input terminal of said input/output terminal; and

a third transistor having said second conductivity, a drain region of the third transistor having the second conductivity is electrically connected to said source region of the first transistor having the second conductivity and the drain region of said second transistor having the second conductivity, a source region of the third transistor having the second conductivity is electrically connected to said input terminal of the input/output terminal, a substrate of the third transistor having the second conductivity is electrically connected to ground, a drain region of the second transistor having the first conductivity, a source region of said second transistor having the second conductivity, a gate of the third transistor having the first conductivity and a gate of the third transistor having the second conductivity are electrically connected to said output terminal of said Schmitt Trigger circuit, said output terminal of the Schmitt Trigger circuit is electrically connected to said input terminal of the second inverter.

9. A power-on bias circuit according to claim 8, wherein said first transistor having the first conductivity, said second transistor having the first conductivity and said third transistor having the first conductivity are each a first P-type transistor, a second P-type transistor and a third P-type transistor; respectively, said first transistor having the second conductivity, said second transistor having the second conductivity and said third transistor having the second conductivity are each a first N-type transistor, a second N-type transistor and a third N-type transistor; respectively.

10. A power-on bias circuit comprising:

a first inverter having an input terminal and an output terminal, said input terminal of the first inverter functions as a first voltage input terminal for said power-on bias circuit;

a second inverter having an input terminal and an output terminal, wherein said output terminal of said second inverter functions as an output terminal for said power-on bias circuit; and

a Schmitt Trigger circuit comprising:

a first P-type transistor;

a second P-type transistor, wherein a substrate of said second P-type transistor, a substrate and a source region of said first P-type transistor are electrically connected to a second voltage input terminal of said power-on bias circuit, a source region of the second P-type transistor is electrically connected to a drain region of said first P-type transistor;

a first N-type transistor;

a second N-type transistor, a gate of said first P-type transistor, a gate of said second P-type transistor, a gate of said first N-type transistor and a gate of said second N-type transistor are electrically connected to said input terminal for said Schmitt Trigger circuit, said input terminal of the Schmitt Trigger circuit is electrically connected to said output terminal of said first inverter, a substrate of said second N-type transistor, a substrate and a source region of said first N-type transistor are electrically connected to ground, a drain region of said second N-type transistor is electrically connected to a source region of said first N-type transistor;

a third P-type transistor, a source region of said third P-type transistor is electrically connected to said drain region of the first P-type transistor and said source region of

the second P-type transistor, a drain region of said third P-type transistor is electrically connected to ground, a substrate of said third P-type transistor is electrically connected to said second voltage input terminal of said power-on bias circuit; and

a third N-type transistor, a drain region of said third N-type transistor is electrically connected to a source region of said first N-type transistor and a drain region of said second N-type transistor, a source region of said third N-type transistor is electrically connected to said second voltage input terminal of said power-on bias circuit, a substrate of said third N-type transistor is electrically connected to ground, a drain region of said second P-type transistor, a source region of said second N-type transistor, a gate of said third P-type transistor and a gate of said third N-type transistor are electrically connected to said output terminal of the Schmitt Trigger circuit, said output terminal of the Schmitt Trigger circuit is electrically connected to said input terminal of the second inverter.

11. A power-on bias circuit according to claim 10, wherein said first inverter comprises a fourth P-type transistor and a fourth N-type transistor, a substrate and a source region of said fourth P-type transistor is electrically connected to said second voltage input terminal of the power-on bias circuit, a drain region of said fourth N-type transistor is electrically connected to ground, a gate of said fourth P-type transistor and a gate of said fourth N-type transistor are electrically connected to said input terminal of said first inverter, a drain region of said fourth P-type transistor and a source region of said fourth N-type transistor are electrically connected to said output terminal of said first inverter.

12. A power-on bias circuit according to claim 10, wherein said second inverter comprises a fourth P-type transistor and a fourth N-type transistor, a substrate and a source region of said fourth P-type transistor is electrically connected to said second voltage input terminal of the power-on bias circuit, a drain region of said fourth N-type transistor is electrically connected to ground, a gate of said fourth P-type transistor and

a gate of said fourth N-type transistor are electrically connected to said output terminal of said second inverter.

13. A power-on bias circuit according to claim 10, wherein said first voltage input terminal of the power-on bias circuit is a core voltage input terminal, said second voltage input terminal of the power-on bias circuit is an input terminal of an input/output terminal.

14. A method for operating a power-on bias circuit comprising the steps of:

providing a first inverter having an input terminal and an output terminal, said input terminal of the first inverter functions as a first voltage input terminal of said power-on bias circuit;

providing a second inverter having an input terminal and an output terminal, wherein said output terminal of said second inverter functions as an output terminal for said power-on bias circuit;

providing a Schmitt Trigger circuit comprising:

a first P-type transistor;

a second P-type transistor, wherein a substrate of said second P-type transistor, a substrate and a source region of said first P-type transistor are electrically connected to a second voltage input terminal of said power-on bias circuit, a source region of the second P-type transistor is electrically connected to a drain region of said first P-type transistor;

a first N-type transistor;

a second N-type transistor, a gate of said first P-type transistor, a gate of said second P-type transistor, a gate of said first N-type transistor and a gate of said second N-type transistor are electrically connected to said input terminal for said Schmitt Trigger circuit, said input terminal of the Schmitt Trigger circuit is electrically connected to said output terminal of said first inverter, a substrate of said second N-type transistor, a substrate and a source region of said first N-type transistor are electrically connected to ground, a drain region of said second N-type transistor is electrically connected to a source region of said first N-type transistor;

a third P-type transistor, a source region of said third P-type transistor is electrically connected to said drain region of the first P-type transistor and said source region of

the second P-type transistor, a drain region of said third P-type transistor is electrically connected to ground, a substrate of said third P-type transistor is electrically connected to said second voltage input terminal of said power-on bias circuit;

a third N-type transistor, a drain region of said third N-type transistor is electrically connected to a source region of said first N-type transistor and a drain region of said second N-type transistor, a source region of said third N-type transistor is electrically connected to said second voltage input terminal of said power-on bias circuit, a substrate of said third N-type transistor is electrically connected to ground, a drain region of said second P-type transistor, a source region of said second N-type transistor, a gate of said third P-type transistor and a gate of said third N-type transistor are electrically connected to said output terminal of the Schmitt Trigger circuit, said output terminal of the Schmitt Trigger circuit is electrically connected to said input terminal of the second inverter;

inputting a first voltage signal into said second voltage input terminal, inputting a second voltage signal into said second voltage input terminal, said first voltage signal is high potential while said second voltage signal is low potential,

outputting a third voltage signal of high potential from said output terminal of the first inverter into said Schmitt Trigger circuit, turning on said first N-type transistor, said second N-type transistor and said third P-type transistor in said Schmitt Trigger circuit, turning off said first P-type transistor, said second P-type transistor and said third N-type transistor, outputting a fourth voltage signal to said second inverter from said output terminal of the Schmitt Trigger circuit, said fourth voltage signal is low potential, outputting a fifth voltage signal from said second inverter after receiving said fourth voltage signal as an output signal from said power-on bias circuit, said fifth voltage signal is high potential; and

inputting said first voltage signal into said second voltage input terminal, inputting said second voltage signal into said second voltage input terminal, wherein said first voltage signal and said second voltage signal are high potential, outputting said third voltage signal of low potential from said output terminal of the first inverter into said Schmitt Trigger circuit, turning on said first P-type transistor, said second P-type transistor and said third N-type transistor in said Schmitt Trigger circuit, turning off said first N-type transistor, said

second N-type resistor and said third P-type transistor, outputting said fourth voltage signal from said output terminal of the Schmitt Trigger circuit into said second inverter, said fourth voltage signal is high potential, outputting said fifth voltage signal from said second inverter after receiving said fourth voltage signal as an output for said power-on bias circuit, said fifth voltage signal is low potential.

15. A method for operating a power-on bias circuit according to claim 14, wherein said first inverter comprises a fourth P-type transistor and a fourth N-type transistor, a substrate and a source region of said fourth P-type transistor are electrically connected to said second voltage input terminal, a drain region of said fourth N-type transistor is electrically connected to ground, a gate of said fourth P-type transistor and a gate of said fourth N-type transistor are electrically connected to said input terminal of the first inverter, a drain region of said fourth P-type transistor and a source region of said fourth N-type transistor are electrically connected to said output terminal of the first inverter.

16. A method for operating a power-on bias circuit according to claim 14, wherein said second inverter comprises a fourth P-type transistor and a fourth N-type transistor, a substrate and a source region of said fourth P-type transistor are electrically connected to said second voltage input terminal, a drain region of said fourth N-type transistor is electrically connected to ground, a gate of said fourth P-type transistor and a gate of said fourth N-type transistor are electrically connected to said input terminal of the second inverter, a drain region of said fourth P-type transistor and a source region of said fourth N-type transistor are electrically connected to said output terminal of the second inverter.

17. A method for operating a power-on bias circuit according to claim 14, wherein said first voltage input terminal is a core voltage input terminal, said second voltage input terminal is an input terminal for said input/output terminal.